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#5 ((fpga asic)<in>metadata)

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1. **FPGA synthesis using Look-Up Table and Multiplexor Based architecture**
Macii, E.; Poncino, M.;
Electrotechnical Conference, 1994. Proceedings., 7th Mediterranean
12-14 April 1994 Page(s):302 - 305 vol.1
Digital Object Identifier 10.1109/MELCON.1994.381090
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2. **A high level design solution for FPGA's**
Makhijani, H.; Meier, S.;
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27-29 Sept. 1994 Page(s):596 - 603
Digital Object Identifier 10.1109/WESCON.1994.403530
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3. **The Exemplar Logic synthesis system: a logic synthesis tool for field pro arrays**
Ligthart, M.; Ranauro, R.;
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23-27 Sept. 1991 Page(s):P13 - 2/1-4
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4. **A hierarchical functional structuring and partitioning approach for multip implementations**
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10-14 Nov. 1996 Page(s):638 - 643
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24-28 Oct. 1995 Page(s):700 - 702
Digital Object Identifier 10.1109/ICSICT.1995.503532
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7. **Algorithm for phase accumulator synthesis for applications in DDS**
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26-28 July 1999 Page(s):210 - 213
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8. **Rapid prototyping and synthesis of a self-testing ABS controller using C/**
Hold, B.; Bhatt, P.C.P.; Agarwal, V.K.;
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21-22 July 1994 Page(s):151 - 156
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9. **FSM synthesis on FPGA architectures**
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10. **Co-synthesis with custom ASICs**
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11. **Use of VHDL synthesis in an advanced digital design course**
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13. **Acceleration of DAB chipset development by deployment of a real-time r**
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Speitel, M.; Schlicht, M.; Leyh, M.;
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1. **VERL: an ontology framework for representing and annotating video eve**
Francois, A.R.J.; Nevatia, R.; Hobbs, J.; Bolles, R.C.; Smith, J.R.;
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Volume 12, Issue 4, Oct.-Dec. 2005 Page(s):76 - 86
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2. **Guest Editor's Introduction: What's New with MPEG?**
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3. **An enhanced LQ adaptive VAr unit controller for power system damping**
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5. **TDAT-time domain analysis tool for EEG analysis**
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Volume 37, Issue 8, Aug. 1990 Page(s):803 - 811
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Trudnowski, D.J.; Smith, J.R.; Short, T.A.; Pierre, D.A.;
Power Systems, IEEE Transactions on
Volume 6, Issue 1, Feb. 1991 Page(s):118 - 126
Digital Object Identifier 10.1109/59.131054

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☐ 1. **Low power methodology and design techniques for processor design**
Brennan, J.P.; Dean, A.; Kenyon, S.; Ventrone, S.;
Low Power Electronics and Design, 1998. Proceedings. 1998 International Syr
10-12 Aug 1998 Page(s):268 - 273

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☐ 2. **A 32b 66 MHz 1.8 W microprocessor**
Bechade, R.; Flaker, R.; Kauffmann, B.; Kenyon, S.; London, C.; Mahin, S.; Ng D.; Roberts, A.; Ventrone, S.; VonReyn, T.;
Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSC(International
16-18 Feb. 1994 Page(s):208 - 209
Digital Object Identifier 10.1109/ISSCC.1994.344667

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1 Lfm2000 - Fifth NASA Langley Formal Methods Workshop

Holloway C. M.

June 2000 Technical Report

Publisher: NASA Langley Technical Report Server

Full text available: pdf(3.71 MB) Additional Information: full citation, abstract

This is the proceedings of Lfm2000: Fifth NASA Langley Formal Methods Workshop. The workshop was held June 13-15, 2000, in Williamsburg, Virginia. See the web site http://shemesh.larc.nasa.gov/lfm2000/ for complete information about the event.

2 A hybrid ASIC and FPGA architecture

Paul S. Zuchowski, Christopher B. Reynolds, Richard J. Grupp, Shelly G. Davis, Brendan Cremen, Bill Troxel

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

Full text available: pdf(116.55 KB) Additional Information: full citation, references, citings, index terms

3 Reconfigurable Computing for Digital Signal Processing: A Survey

Russell Tessier, Wayne Burleson

May 2001 **Journal of VLSI Signal Processing Systems**, Volume 28 Issue 1-2

Publisher: Kluwer Academic Publishers

Full text available: Publisher Site Additional Information: full citation, abstract, citings

Steady advances in VLSI technology and design tools have extensively expanded the application domain of digital signal processing over the past decade. While application-specific integrated circuits (ASICs) and programmable digital signal processors (PDSPs) remain the implementation mechanisms of choice for many DSP applications, increasingly new system implementations based on *reconfigurable computing* are being considered. These flexible platforms, which offer the functional efficienc ...

Keywords: FPGA, reconfigurable computing, signal processing, survey

4 Recent developments in high-level synthesis

Youn-Long Lin

January 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available: pdf(232.47 KB) Additional Information: full citation, abstract, references, citings, index terms

We survey recent developments in high level synthesis technology for VLSI design. The need for higher-level design automation tools are discussed first. We then describe some basic techniques for various subtasks of high-level synthesis. Techniques that have been proposed in the past few years (since 1994) for various subtasks of high-level synthesis are surveyed. We also survey some new synthesis objectives including testability, power efficiency, and reliability.

Keywords: VLSI design, design automation, design methodology, high level synthesis

5 Design and Implementation of Viterbi Decoder with FPGAs

M. Kivioja, J. Isoaho, L. Vänskä

May 1999 **Journal of VLSI Signal Processing Systems**, Volume 21 Issue 1

Publisher: Kluwer Academic Publishers

Full text available: Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper we present our studies for implementing complex DSP and Telecom systems in FPGAs. We analyse suitability of FPGA device architectures for implementing complex algorithms. Here we use a Viterbi algorithm as a deeper case study. Different architectural strategies for implementations are discussed and analysed with the special emphasis on practical FPGA implementations. Speed performance, easy routability and minimisation of inter-chip communication are used as design criter ...

6 Synthesis of application-specific highly efficient multi-mode cores for embedded systems

Lih-yih Chiou, Swarup Bhunia, Kaushik Roy

February 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 1

Publisher: ACM Press

Full text available: pdf(321.54 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present a novel design methodology for synthesizing multiple configurations (or modes) into a single programmable core that can be used in embedded systems. Recent portable applications require reconfigurability of a system along with efficiency in terms of power, performance, and area. The field programmable gate arrays (FPGAs) provide a reconfigurable platform; however, they are slower in speed with significantly higher power and area than achievable by a customized applicati ...

Keywords: Digital signal processing (DSP), application specific integrated circuits (ASIC), embedded systems, high level synthesis, reconfigurable system, synthesis

7 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Publisher: ACM Press

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

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L11	219	partitioning same synthesis and hybrid	US-PGPUB; USPAT	OR	ON	2005/12/23 13:45
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L14	92	partitioning same synthesis and fpga and interconnect	US-PGPUB; USPAT	OR	ON	2005/12/23 14:01
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L30	14	partitioning same (interconnect or signal or vector) same (extension or prefix or suffix or thread) and programmable and synthesis	US-PGPUB; USPAT; DERWENT; IBM_TDB	OR	ON	2005/12/23 14:40

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L3	259	fpga same asic and hybrid and synthes$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 22:07
L2	544	716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 21:17
S18 6	69	fpga same standard adj cell and file and synthes$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 20:47
S18 7	2	"20040268288"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 19:39
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S18 4	1	fpga adj2 file same standard adj cell same file and synthes$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 15:50
S18 3	32	hybrid same fpga same asic same (chip til$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 15:48
S18 1	2	"6779156".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 15:41

S170	2	"5995730".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 15:23
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S165	157	S163 and S164	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 12:30
S164	1030	(rtl $hdl hardware adj2 language) and (fpga same (asic standard adj cell))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 12:30

S163	225062	(signal interconnect$3 connect$3 wir$3) adj2 (type group)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 12:28
S161	205	($HDL rtl) same (prefix extension) and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:20
S160	12	fpga same (asic standard adj cell) same ($HDL rtl) same (prefix extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:19
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S158	5	fpga same asic same rtl same (prefix extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:18
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S156	0	hybrib same fpga same asic and (prefix suffix extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:16
S155	0	hybrib same fpga same asic same (prefix suffix extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:16

S154	360	fpga same (cell asic) and (rtl $HDL verilog hardware near4 language) and (interconnect$3 connect$3 wir$3) and (prefix suffix extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:15
S152	19	hybrid same fpga same asic and (rtl $HDL verilog hardware near4 language) and (interconnect$3 connect$3 wir$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:08
S151	20	hybrid same fpga same asic and (rtl $HDL verilog hardware near4 language)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:07
S150	177	hybrid same fpga same asic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 11:05
S149	1	(FPGA PLD) same interconnect$3 same ($HDL RTL) and (standard adj cell) and til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 10:32
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S148	2	($HDL rtl hardware near4 language) same (interconnect$3 connect$3 wir$3) same (extension prefix suffix) same (fpga pld programmable adj2 device) and (synthes$6 partition$3 map$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 10:30
S147	604	($HDL rtl hardware near4 language) and (interconnect$3 connect$3 wir$3) and (extension prefix suffix) and (fpga pld programmable adj2 device) and (synthes$6 partition$3 map$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 10:29

S132	4	rtl same fpga same cell same cod$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 09:48
S131	2	rtl same fpga same standard adj2 cell same cod$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/23 09:47
S130	76	(rtl $HDL verilog) and (extension prefix suffix) and (interconnect$3 connect$) and FPGA and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 18:03
S129	3	(rtl $HDL verilog) same (extension prefix suffix) same interconnect$3 and FPGA and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 18:02
S128	18	(rtl $HDL verilog) same (extension prefix suffix) same interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 18:02
S122	5416	(rtl $HDL verilog) and (extension prefix suffix)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:59
S127	47	S125 and S121 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:57
S126	567	S125 and S121	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:57

S125	1725	(rtl $HDL verilog description adj language) and (prefix suffix)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:56
S124	147	S123 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:05
S123	1273	S121 and S122	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:05
S120	160	(rtl $HDL verilog) same extension and ((interconnect$3 connect$3) with (type or group$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:04
S121	1095846	((interconnect$3 connect$3) with (type or group$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 17:03
S32	727234	(rtl rt (register adj transfer) $HDL (high adj level) (hardware adj description adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 16:57
S119	2	"20040044971"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 09:22
S118	2	"6859914"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 09:22

S117	2	"20030177454"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/22 09:14
S116	134	(rtl $hdl verilog high adj definition adj language)and extension and fpga and partition$3 and ((interconnect$3 connect$3) with type)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 19:59
S8	99	logic adj design same (RTL (register adj transfer$3 adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 19:45
S104	135	rtl and fpga and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/18 17:51
S103	543	716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/18 17:03
S102	135	rtl and fpga and standard adj cell and (net interconnect$3 connect$3 wir$3 rout$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 16:48
S101	135	rtl and fpga and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 16:47
S100	2	"20040068331"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 16:46

S99	145	extension and (interconnect$3 connect$3)same ($HDL RTL)and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 16:27
S98	8	extension same (interconnect$3 connect$3)same ($HDL RTL)and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:39
S97	291	extension same (interconnect$3 connect$3)same ($HDL RTL)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:33
S96	1453	extension same (interconnect$3 connect$3)and ($HDL RTL)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:33
S95	169	extension same interconnect$3 and ($HDL RTL)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:32
S94	8	extension same interconnect$3 same RTL	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:20
S93	6	language adj extension same interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:20
S92	514	language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/16 15:18
S91	1	"5278769".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44
S90	1	"5278769".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44

S89	1	"5111413".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44
S88	1	"5111413".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44
S87	1	"5463563".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44
S86	1	"5452227".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:44
S85	1	"5452226".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:43
S84	1	"5423023".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:43
S83	1	"5452226".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:43
S82	1	"5423023".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:43
S81	1	"5423023".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:43
S80	1	"5423023".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:42
S79	1	"5384710".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:42
S78	1	"5384710".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:42
S77	1	"5278769".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:41
S76	1	"5263162".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:41
S75	1	"5084824".PN.	USPAT; USOCR	OR	ON	2005/12/15 12:40
S74	3	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix) and dynamic$4 near4 model$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:37
S73	2	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix) and dynamic$4 adj model$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:37
S72	17	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:36

S71	2	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix) and 716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:16
S70	2	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix)and file and 716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:16
S69	89	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix)and file	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:14
S68	15	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (suffix)and file	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:14
S67	89	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same (extension suffix)and file	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:13
S66	74	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same extension and file	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:10
S55	291	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:02
S54	2	"6574787".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:01

S53	2	"6477697".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 12:01
S64	105	S58 and S59 and S60 and S61	US-PGPUB; USPAT	OR	ON	2005/12/15 11:59
S65	15	SIM and xilinx.as.	US-PGPUB; USPAT	OR	ON	2005/12/15 11:54
S63	113	S58 and S59 and S60	US-PGPUB; USPAT	OR	ON	2005/12/15 11:54
S62	116	S58 and S59	US-PGPUB; USPAT	OR	ON	2005/12/15 11:01
S61	4941824	(partition$3 group$3 cluster$3 divid$3 subdivid$3 subpartition$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 10:59
S60	8183324	(type or class or category or group$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 10:58
S59	54578	(interconnect$3 connect$3) and (FPGA or (programmable near3 device) or PLD)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 10:57
S58	776	(RTL register adj transfer adj language $HDL verilog high adj definition adj language) same extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 10:55
S1	15	(FPGA PLD) same standard same interconnect$3 same ($HDL RTL)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/15 10:51
S57	14	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) and extension adj language and (FPGA PLD progammable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 20:31

S56	10	(interconnect$3 connect$3) same ($HDL RTL (high adj definition adj language) (register adj transfer adj level)) same extension and (FPGA PLD progammable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 20:30
S52	2	"6769107".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 17:08
S51	2	"20050149898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 16:59
S49	67	S44 same S45 and G06F017$.IPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:24
S35	661	S33 same S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:23
S47	1	S44 same S45 and extension	DERWENT; IBM_TDB	OR	ON	2005/12/14 13:22
S46	1	S44 same S45 and extension	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:22
S45	60869	(partition$3 group$3 cluster$8 divid$3 subdivid$3 subpartition$3) same S42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:19
S44	1821	S42 same S43	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:19

S43	727234	(rtl rt (register adj transfer) $HDL (high adj level) (hardware adj description adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:19
S42	190480	(interconnect$3 connect43 wire wiring route routing net) near5 (type class$8 category group$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 13:19
S40	22	S33 same S34 and extension and 716/1-18.ccls.	US-PGPUB; USPAT	OR	ON	2005/12/14 13:19
S41	2694042	"31" and "32"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 12:26
S31	190480	(interconnect$3 connect43 wire wiring route routing net) near5 (type class$8 category group$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 12:26
S39	193	S33 same S34 and extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 11:02
S38	1	S35 same S36 and 716/1-18.ccls.	US-PGPUB; USPAT	OR	ON	2005/12/14 11:00
S37	11	S35 same S36	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 11:00
S36	310350	(FPGA (programmable adj2 (array or device)) PGA PLD CPLD antifuse fuse)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 10:58
S34	60869	(partition$3 group$3 cluster$8 divid$3 subdivid$3 subpartition$3) same S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 10:55

S33	1821	S31 same S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 10:53
S30	50	(RTL or (register adj transfer adj language) $HDL "Verilog") same (interconnect connect wir$3) near5 type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 10:48
S20	1425	(RTL or register adj transfer adj language) same (interconnect connect wir$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:25
S29	22	S20 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:21
S28	7628	(interconnect connect wir$3) near5 signal with type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:21
S23	201460	(interconnect connect wir$3) near5 signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:21
S27	4	S25 and S26	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:15
S26	368	(FPGA PLD) same standard near4 cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:15

S25	69	S20 same S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:13
S24	208	S20 and S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:13
S22	2	S20 and S21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:12
S21	474	(interconnect connect wir$3) adj type near5 signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 09:12
S19	2	"20040268288"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 08:59
S18	50	(RTL $HDL (register adj transfer$3 adj language))same extension same (connect interconnect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 18:06
S17	1906	(RTL $HDL (register adj transfer$3 adj language))and extension and (connect interconnect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 18:06
S16	44	(RTL $HDL (register adj transfer$3 adj language))and language adj extension and (connect interconnect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 18:06

S15	46	cod$3 and (RTL (register adj transfer$3 adj language $HDL))and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 18:01
S14	28	logic adj design and (RTL (register adj transfer$3 adj language $HDL))and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 18:00
S13	34	logic adj design and (RTL (register adj transfer$3 adj language $HDL))and extension near3 language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:57
S12	3	logic adj design same (RTL (register adj transfer$3 adj language))and extension near3 language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:54
S11	9	logic adj design same (RTL (register adj transfer$3 adj language))and extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:53
S10	5	logic adj design same (RTL (register adj transfer$3 adj language))and FPGA and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:51
S9	23	logic adj design same (RTL (register adj transfer$3 adj language))and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:47
S7	6331	logic adj design	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:46

S6	1	(FPGA) same interconnect$3 same ($HDL RTL) and (standard adj cell) and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:45
S5	1	(FPGA) same interconnect$3 same ($HDL RTL) and (standard adj cell) and file and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:44
S4	15	(FPGA PLD) same interconnect$3 same ($HDL RTL) and (standard adj cell) and file	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:44
S2	22	(FPGA PLD) same interconnect$3 same ($HDL RTL) and standard adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/13 17:30